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A study on the electrical properties of plasma nitrided oxide gate dielectric in flash memory

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In this paper, we address the effect of plasma nitridation on the gate dielectric in terms of device characteristics of an NMOS/PMOS transistor. Firstly, boron segregation due to plasma nitridation near Si/SiO_2 interface and bulk Si is experimentally characterised by 1D SIMS, and its profile is reproduced in simulation of which parameters for boron diffusion are accurately calibrated through a comprehensive calibration process. Secondly, the electrical behaviour of NMOS/PMOS transistor with plasma nitride gate dielectric is verified, observing uncommon behaviour of C-V diagram in the case of buried-channel PMOS transistor. We prove that an excessive amount of interface traps generated by plasma nitridation influence abnormal electrical behaviour of the NMOS/PMOS transistor.

Keywords: dry oxidation; plasma nitridation; process simulation; boron segregation; C-V diagram

1. Introduction

Plasma nitridation provides strong immunity to boron penetration of p^+ poly gate and incorporates nitrogen (N) atoms at the Si/SiO_2 interface which improves hot carrier resistance, leakage current and stress immunity. These principal advantages of plasma nitrided gate dielectric over conventional oxynitridation with NO or N_2O have motivated much work on its utilisation, and plasma nitridation is now regarded as a promising technology for a reliable gate insulator for electrical erasable nonvolatile memory such as flash memory [1,2]. However, there remain many issues to be addressed if its electrical characteristics are considered [3]. One of the issues is the dopant segregation of additional annealing process of plasma nitridation, which changes the electrical property of cells and peripheral transistors. Another problem is the effect of the positive charge trap mainly generated in Si/SiO_2 interface where ion damage of plasma nitridation is maximised.

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In this paper, we address the effect of plasma nitridation on the gate dielectric by combined experimental and simulation study of gate oxidation.

2. Experiments and simulations

Samples needed for this study are fabricated with the same process for the fabrication of 63 nm NAND flash cell transistor [4]. BF_2 dose ($7 \times 10^{12}cm^{-2}$) for NMOS transistor and BF_2 dose ($1 \times 10^{13}cm^{-2}$) for PMOS transistor are implanted separately at low energy (20 KeV) through a screen oxide. After the screen oxide removal, gate oxidation is performed to grow 80 A oxide with temperature of 900°C for 60 minutes. Poly-Silicon is used as gate material and aluminum is used for metal electrode.

2.1. *Boron segregation*

First, boron segregation at the Si/SiO_2 interface and boron diffusion in silicon surface are experimentally characterised by means of 1D SIMS. Samples with various gate oxidations are prepared with the same process conditions as listed in Table 1. After growing gate dielectric by dry oxidation, NO anneal and plasma nitridation are applied to several samples selectively. Boron segregation acquired by high-resolution 1D SIMS is depicted in Figure 1. It is seen that the boron concentration profile is changed when NO anneal is added while plasma nitridation has no effect on the profile. Thus, it is confirmed that plasma nitrided gate dielectric possesses the same boron concentration profile on Si as the gate dielectric with dry oxidation.

Table 1. Samples used to study segregation during gate oxidation.

Sample	Oxidation	Plasma nitridation
SA1	Dry oxidation	X
SA2	Dry oxidation	O
SA3	Dry oxidation + NO anneal	X
SA4	Dry oxidation + NO anneal	O

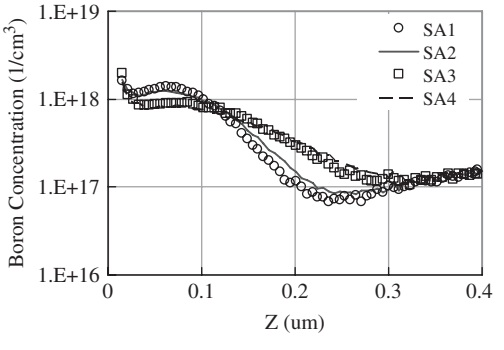

Figure 1. SIMS profiles for samples with gate oxidation.

2.2. *3-D simulation calibration*

Secondly, a comprehensive process simulation model is accurately calibrated and then exploited to investigate the dependence of device electrical parameters on NMOS/PMOS transistors. As shown in Figure 2, 2-D and 3-D process simulation are performed with ENEXSS tools and device simulation is performed with Synopsys tools [5]. For accurate simulation, critical physical dimensions such as length/width of transistor and tunnel oxide thickness are measured by SEM and TEM. To extract process simulation model parameters (boron segregation, oxidation enhanced diffusion (OED) and transient enhanced diffusion (TED)), a variety of NMOS/PMOS transistors with different lengths and widths are tested. After the calibration, we obtained Id-Vg profiles of NMOS/PMOS transistor with different length as shown in Figure 3. It is seen that I_{ON}, I_{OFF} and V_{TH} are correctly simulated on both the length of 0.3 μm and 20 μm. Based on these calibration results, boron concentration profile in Si is constructed as shown in Figure 4. Since the calibration is performed with typical dry oxidation models while neglecting the effect of plasma nitridation, we compare the boron profile of a SA3 sample for a start. The simulation profile shows a good match to SIMS data in Si, confirming the accuracy of the calibration. Since the 3-D simulation has different material on top of the Si/SiO2 interface, the boron profile near Si/SiO_2 the interface is different when compared to SIMS data.

For identifying the electrical characteristics of plasma nitrided gate dielectric, Id-Vg curves for the LVN/LVP transistor are measured experimentally and compared as shown in Figure 5. While both samples possess the same boron concentration profile in Si, V_{TH} of NMOS and PMOS transistor of plasma nitrided gate oxide is 0.1 V lower than the sample of dry oxidation. Furthermore, in a C-V diagram of each sample as shown in Figure 6, it is

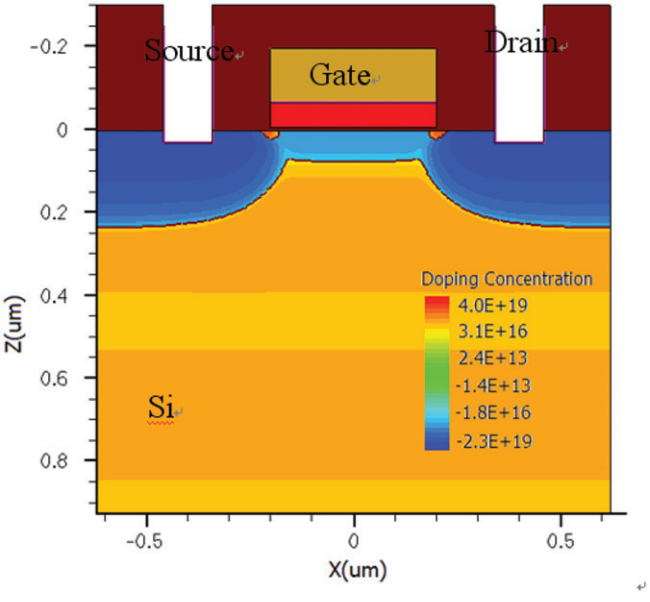

Figure 2. Doping concentration of PMOS transistor constructed by 2-D process simulation.

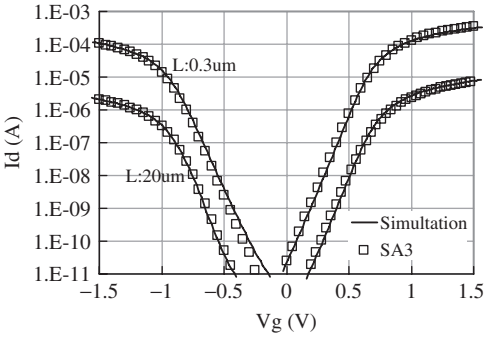

Figure 3. Id-Vg profiles of SA3 (NO annealed gate dielectric) sample for LVN and LVP transistor. Length dependency is shown well fitted due to the calibration of process simulation parameters.

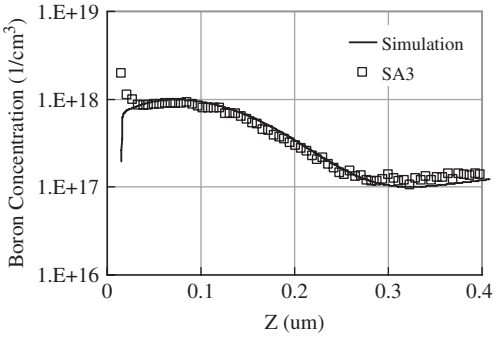

Figure 4. SIMS profile of SA3 sample and calibrated simulation result near Si/SiO_2 interface.

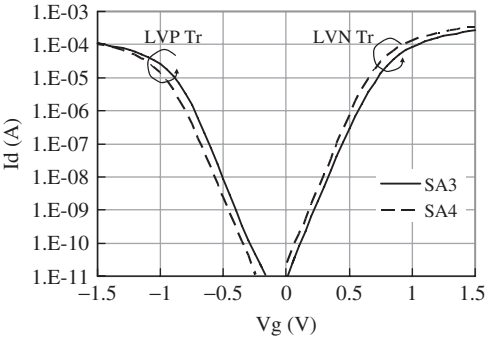

Figure 5. Id-Vg profiles for LVN and LVP transistor. SA4 sample (plasma nitrided gate dielectric) possesses 0.1 V lower V_{TH} value than SA3 sample.

observed that uncommon peak near $Vg = 0\,V$ on a buried channel PMOS capacitor exists in the case of plasma nitrided gate dielectric. These results indicate that plasma nitridation alters the physical property in bulk SiO_2 and Si/SiO_2 surface and changes the electrical characteristics of the NMOS/PMOS transistor.

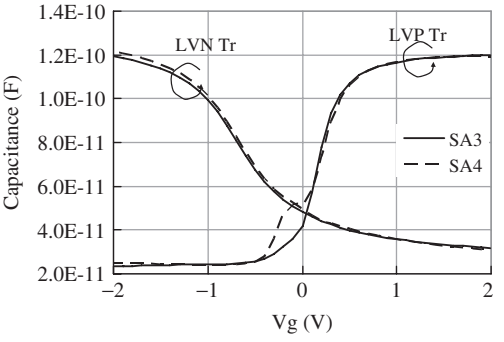

Figure 6. C-V profiles of surface channel NMOS and buried channel PMOS capacitors with different gate oxidation conditions. Buried channel PMOS capacitor of SA4 exhibits uncommon shape near Vg = 0 V.

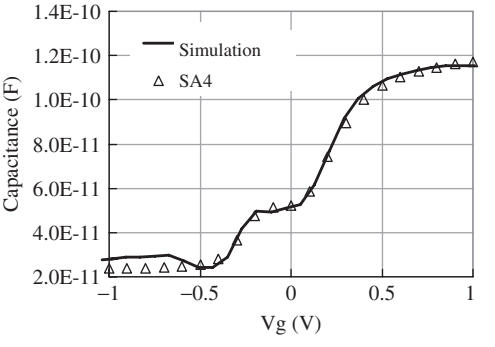

Figure 7. C-V profile for buried channel PMOS capacitor with SA4 sample and calibrated simulation result. Nit value equals 9E11 which is three times higher than that of SA3 sample.

2.3. *C-V diagram of plasma nitrided oxide*

For the purpose of identifying the reason for 0.1 V difference in Id-Vg curve and abnormal peak in C-V diagram, we utilise 3-D simulation. In 3-D simulation, we added several oxide bulk traps and interface traps into the SiO_2 and Si/SiO_2 interface deliberately, and then observed their device characteristics. As shown in Figure 7, the C-V curve is reproduced by adding an excessive amount of interface trap in Si/SiO_2 interface. The amount of interface trap was measured to be 9e11 which is three times higher than that of dry oxidation. The excessive trap located near interface is regarded as the evidence of positive charge trap of the plasma nitrided gate dielectric [1,2]. The uncommon peak near Vg = 0 V in the C-V diagram illustrates V_{TH} shift by electron trap/detrap of the trap sites in gate dielectric and appears clearly on the buried channel PMOS capacitor since its C-V curve changes mainly under inversion conditions with abundant supply of electrons from N-Well [6,7]. Whereas, the surface channel NMOS capacitor shows little change since its C-V curve changes under the depletion condition with few electrons on the Si surface. While oxide bulk trap possesses the same effect on the shift of Id-Vg curve as interface trap, it has no influence on

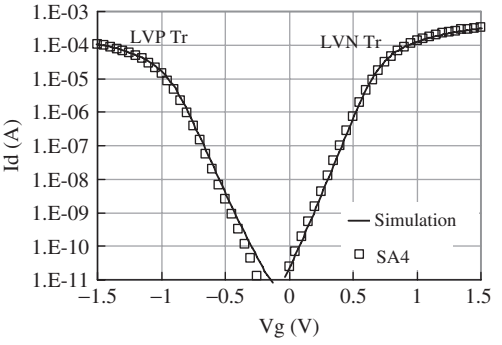

Figure 8. Id-Vg profiles for surface channel NMOS and buried channel PMOS transistor of SA4 sample. Simulation results with N_{IT} value of 9E11 show good agreement with experiments.

abnormal peak of the C-V diagram. Based on these process and device simulation parameters, Id-Vg characteristics of NMOS and PMOS transistor with plasma nitrided gate dielectric are obtained by the device simulation as shown in Figure 8. It shows good agreement with experimental data, confirming that 0.1 V V_{TH} shift was attributed by positive charge trap of the plasma nitrided gate dielectric.

3. Conclusions

The effect of plasma nitridation on the gate dielectric in terms of device characteristics is investigated through simulations and experiments. First, based on accurate calibration of 3-D simulation, it is verified that plasma nitridation has no effect on boron segregation near the Si/SiO_2 interface and bulk Si. Secondly, we observe uncommon behaviour of the C-V diagram in the case of buried-channel PMOS transistor. We prove that it is due to an excessive amount of interface traps generated by plasma nitridation.

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